REMARKS

Claims 1-6 have been amended to conform to U.S. practice and to eliminate multiple dependent claims. New claims 7-20 have been added.

Now pending in this application are claims 1-7, 8-15, and 16-20. Of these, claims 1, 8, and 16 are independent.

Attached is a marked-up version of the changes being made by the current amendment.

Applicant asks that all claims be examined. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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Version with markings to show changes made

In the claims:

Claims 1-6 have been amended as follows:

1. (Once amended) A method for fabricating a contact hole for a semiconductor memory component, [in particular a DRAM or an FRAM], having a silicon substrate, an intermediate dielectric layer [(1)] arranged on said substrate, and an upper layer [(3) made of a ferroelectric material or made of a material having a high dielectric constant being] arranged on said intermediate dielectric layer, [having the steps of] the method comprising:

f[F]orming a perforated mask on the upper layer [(3)], the mask including a material which exhibits temperature stability during a later deposition process [being used for the perforated mask];

e[E]tching the upper layer [(3)] and a depression [(8')] into the intermediate dielectric layer [(1)] as far as a residual thickness [(d_0)] using the perforated mask;

d[D]epositing a layer [made of] including O_3/TEOS-SiO_2 onto [the] a structure thus obtained including the perforated mask [in the later deposition process];

r[R]emoving the layer [made of] including O_3/TEOS-SiO_2 from [the] a bottom of the depression [(8')] by etching; and

t[T]hereupon lowering the depression [(8')] by etching in order to produce the contact hole as far as [the] an interface with the silicon substrate, the [latter] silicon substrate being uncovered, the layer [made of] including O_3/TEOS-SiO_2 serving as a lateral seal of the upper layer [(3)] during the [etching process] lowering of the depression.

2. (Once amended) The method as claimed in claim 1, wherein [polyimide is used as the material for] forming the perforated mask comprises forming a perforated mask including polyimide.

3. (Once amended) The method as claimed in claim 1, wherein [photoimide is used as the material for] forming the perforated mask comprises forming a perforated mask including photoimide.

4. (Once amended) The method as claimed in claim 1, [2 or 3,] wherein, after the uncovering of the silicon substrate [in the region of] at the bottom of the contact hole, the [latter] silicon substrate being spared, a second layer [made of] including O_3/TEOS-SiO_2 is [again] deposited [onto this structure] into the contact hole and onto a top surface proximate the contact hole.

5. (Once amended) The method as claimed in claim 4, wherein the perforated mask material is stripped prior to [renewed] deposition of the second layer including O_3/TEOS-SiO_2.

6. (Once amended) The method as claimed in claim 1, [one of the preceding claims, wherein a layer made of] further comprising:

selecting a material for the upper layer from the group consisting of a ferroelectric material [, in particular SBT or PZT, or made of a] and a material having a high dielectric constant[, in particular BST, is used as the upper layer (3)].

In the abstract:

[The invention relates to a method for producing a semiconductor memory element, in particular a DRAM or FRAM. Said memory element comprises a silicon substrate, an intermediate oxide layer (1) applied to the latter, upon which an upper layer (3) consisting of a ferroelectric material or a material with higher dielectric constants is provided. A contact cavity (8) which extends up to the border between the silicon substrate and the upper layer is etched, from the starting point of an opening (5) in a cavity mask which has been configured in a previous stage. A material resistant to high temperatures is used for the cavity mask. Such a material must withstand high temperatures so that the subsequent deposition of O_3-TEOS-SiO_2 onto this layer (for example polymide) can take place, without causing any degradation of said layer. The cavity mask is used for etching into the intermediate oxide layer (1), causing the

formation of a recess (8'). A layer consisting of O_3-TEOS-SiO_2 is then deposited onto the resultant structure. In order to create the contact cavity, the O_3-TEOS-SiO_2 layer is removed from the base of the recess (8') by etching and said recess (8') is then sunk to the border with the silicon substrate by etching, thus exposing the substrate.]

A method for fabricating a contact hole for a semiconductor memory element. The memory element includes a silicon substrate, an intermediate dielectric layer on the substrate, and an upper layer on the intermediate dielectric layer. The method includes forming a perforated mask on the upper layer, the mask including a material that exhibits temperature stability. The upper layer and a depression are etched into the intermediate dielectric layer as far as a residual thickness using the perforated mask. A layer including O_3/TEOS-SiO_2 is deposited onto a structure thus obtained. The layer including O_3/TEOS-SiO_2 is removed from a bottom of the depression by etching. The depression is lowered by etching to produce the contact hole as far as an interface with the silicon substrate, the silicon substrate being uncovered, and the layer including O_3/TEOS-SiO_2 serving as a lateral seal of the upper layer during the lowering of the depression.